SWAMI VIVEKANAND UNIVERSITY, SIRONJA, SAGAR (M.P.)

SCHEME

For

MASTER OF TECHNOLOGY (M.Tech.)

EMBEDDED SYSTEM AND VLSI DESIGN

Course Code : MTVD

Department of Electronics & Communication Engineering

Faculty of Engineering

Duration of Course	:	2 Year
Examination Mode	:	Semester
Examination System	:	Grading

Swami Vivekanand University, Sironja Sagar (M.P.)

2016-2017

Swami Vivekanand University, Sagar (M.P.)
Scheme of Examination

Faculty of Engineering — Department of Electronics & Communication Engineering

Scheme of Course : M.Tech. - Embedded System and VLSI Design. Course Code : MTVD — Semester :- 1st Sem

Paper / Subject Code	Title of the Paper / Subject	Credit Allotted			Total Credit	Distribution of Marks											Duration of Theory Exam
						Theory					Practical					Grand Total (I= D+H)	
						End Sem.		Internal		Total (D= A+B+C)	End Sem.		Internal		Total (H= E+F+ G)		
		L	T	P		Max (A)	Min	MST (B)	TW (C)		Max (E)	Min	LW (F)	PQ (G)			
MTVD-0101	Advanced Mathematics	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0102	CMOS VLSI Design	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0103	Advanced Logic Design	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0104	Digital Signal Processing	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0105	Embedded Microcontroller Programming	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0106	Lab-I Embedded System Design	-	-	6	6	-	-	-	-	-	90	28	-	60	150	150	-
MTVD-0107	Lab-II Digital Design	-	-	6	6	-	-	-	-	-	90	28	-	60	150	150	-
	Total	15	05	12	32	350	-	100	50	500	180	-	-	120	300	800	

SWAMI VIVEKANAND UNIVERSITY SAGAR (M.P.)
Scheme of Examination

Faculty of Engineering — Department of Electronics & Communication Engineering

Scheme of Course : M.Tech. – Embedded System and VLSI Design. Course Code : MTVD — Semester :- 2nd Sem

Paper / Subject Code	Title of the Paper / Subject	Credit Allotted			Total Credit	Distribution of Marks											Duration of Theory Exam
						Theory					Practical					Grand Total (I= D+H)	
						End Sem.		Internal		Total (D= A+B+C)	End Sem.		Internal		Total (H= E+F+ G)		
		L	T	P		Max (A)	Min	MST (B)	TW (C)		Max (E)	Min	LW (F)	PQ (G)			
MTVD-0201	VLSI Technology	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0202	Real Time Operating System	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0203	VLSI Test and Testability	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0204	Microelectronics	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0205	Embedded Computing System Design	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0206	Lab-III Real Time Operative System	-	-	6	6	-	-	-	-	-	90	36	-	60	150	150	3 Hrs
MTVD-0207	Lab-IV VLSI Technology	-	-	6	6	-	-	-	-	-	90	36	-	60	150	150	-
	Total	15	05	12	32	350		100	50	500	180	-	-	120	300	800	

Swami Vivekanand University, Sagar (M.P.)
Scheme of Examination

Faculty of Engineering — Department of Electronics & Communication Engineering

Scheme of Course : M.Tech. - Embedded System and VLSI Design. Course Code : MTVD — Semester :- 3rd Sem

Paper / Subject Code	Title of the Paper / Subject	Credit Allotted			Total Credit	Distribution of Marks											Duration of Theory Exam
						Theory					Practical					Grand Total (I= D+H)	
						End Sem.		Internal		Total (D= A+B+C)	End Sem.		Internal		Total (H= E+F+ G)		
		L	T	P		Max (A)	Min	MST (B)	TW (C)		Max (E)	Min	LW (F)	PQ (G)			
MTVD-0301	Elective I	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0302	Elective II	3	1	-	4	70	28	20	10	100	-	-	-	-	-	100	3 Hrs
MTVD-0303	Seminar	-	-	4	4	-	-	-	-	-	-	-	-	100	100	100	-
MTVD-0304	Preliminary Dissertation cum Synopsis	-	-	8	8	-	-	-	-	-	120	48	-	80	200	200	-
	TOTAL	06	02	12	20	140	-	40	20	200	120	-	-	180	300	500	

Elective –I **MTVD 301 (A)** Opto-Electronics Integrated Circuit

MTVD 301(B) System On Chip (SOC) Design

Elective –II **MTVD 302 (A)** Communication RF IC Design

MTVD 301(B) Embedded system Programming

Swami Vivekanand University, Sagar (M.P.)
Scheme of Examination

Faculty of Engineering — Department of Electronics & Communication Engineering

Scheme of Course : M.Tech. - Embedded System and VLSI Design. Course Code : MTVD — Semester :- 4th Sem

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments /Quiz	End Sem. Practical/Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MEVD 401	Dissertation Part- II	-	-	20	20	-	-	-	300	200	500
		Total	-	-	20	20	-	-	-	300	200	500

L: Lecture - T: Tutorial - P: Practical